

REMARKS

Claims 3 and 8 were objected to under 37 CFR 1.75 as being a substantial duplicate of claim 10. The Examiner further advises that should claims 2, 3 and 4 be found allowable, claims 6, 8 and 9, respectively, will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof.

Claims 6, 7, 8, and 9 were amended to depend on claim 5. The scope of independent claim 5 is different from the scope of independent 1 and therefore claims 6, 8, and 9 are no longer substantial duplications of claims 2, 3, and 4.

Claim 5 was rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claim 5 was amended to overcome the rejection by inserting the word said before the word capping in line 7.

Claims 1, 4, 5, 7 and 9 were rejected under 35 U.S.C. 102(a) as being anticipated by Ohtani; and claims 2 and 6 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani as applied to claims 1, 4, 5, 7 and 9, and further in view of Ishihara.

The examiner bases the rejection of the above claims on the statement that the Ohtani et al. patent discloses providing a silicon substrate 201 with an upper surface; forming an amorphous region (203) is said upper surface by exposing said upper surface to halogen species; and forming a dielectric layer of silicon oxide (209) on said amorphous region; wherein said halogen species is chlorine (See claim 5 and col. 6, lines 30-34). In col. 9, lines 60 – 61 of the Ohtani et al. patent the amorphous film to which the examiner refers (i.e. 203) is deposited at a thickness of from 500 to 1000Å. The deposition process is completely different from the process disclosed and claimed in the instant invention. Claim 5 to which the examiner refers is dependent on claim 1 where the semiconductor film comprises amorphous silicon on an insulating surface of a substrate. Claim 1 further contains the limitation of crystallizing said semiconductor

film and annealing said semiconductor film at a temperature range of 900 to 1200°C. Claim 5 further contains the limitation of annealing in a chlorine containing species. It is well known that a claim should be interpreted in the context of the disclosure. The Ohtani et al. Patent teaches depositing the amorphous layers. As a part of the crystallization process of the amorphous layers the Ohtani et al. patent teaches annealing the films in a chlorine containing species. The Ohtani et al. patent certainly does not teach forming an amorphous layer by exposure to a halogen as described and claimed in the instant invention. Therefore The Ohtani et al. patent is not a valid 102(b) reference as described by the examiner and claims 1, 4, 5, 7, and 9 are allowable over the cited art.

In addition claims 2 and 6 also contain the limitation of forming the amorphous layer by exposure to a halogen. This is not taught or disclosed in the Ohtani et al. patent nor the Ishihara et al. patent and claims 2 and 6 are allowable over the cited art.

Applicant appreciates the indication that claims 10 and 11 are allowed.


In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made.**"

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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Version with Markings to Show Changes Made

5 (Amended). A method for forming an interface between a silicon surface and a dielectric layer comprising:

providing a silicon substrate with an upper surface;

forming an amorphous region in said upper surface by exposing said upper surface to halogen species;

forming a capping layer on said amorphous region; and

forming a dielectric layer on said capping layer.

6 (Twice amended). The method of claim [1] 5 further comprising removing a dielectric layer from said upper surface prior to forming said amorphous region.

7 (Amended). The method of claim [1] 5 wherein said halogen species is selected from the group consisting of chlorine, bromine, iodine and fluorine.

8 (Amended). The method of claim [1] 5 wherein said forming said amorphous further comprises:

exposing a chlorine containing gas to UV radiation to form excited chlorine species;

heating said upper surface to a temperature between 50°C and 250°C; and

exposing said heated upper surface to said excited chlorine species.

9 (Amended). The method of claim [1] 5 wherein said dielectric layer is formed using a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, and a silicate.